

FIG. 1 is a block diagram of a video recording and reproduction apparatus. The apparatus includes a digital interface (30) connected to an IRD (101). It also features an input switch (12) receiving video and audio inputs from a ground wave tuner (11). The video signal path includes a YC separator (13), an input switch (14), an audio A/D converter (19), an MPEG audio encoder (20), a video signal pre-processing section (17), an MPEG video encoder (18), a multi-plexing and demulti-plexing circuit (21), a buffer control section (22), and an HDD (23). The audio signal path includes an NTSC decoder (15), a synchronizing circuit (16), a video signal post-processing section (25), an MPEG AV decoder (24), an NTSC encoder (27), an OSD circuit (26), an audio D/A converter (29), and a switch (28). The system is controlled by a system controller (31) which manages ROM (33), RAM (34), and a DRIVE (111) with data (121), read (122), write (123), and erase (124) operations.

FIG. 1

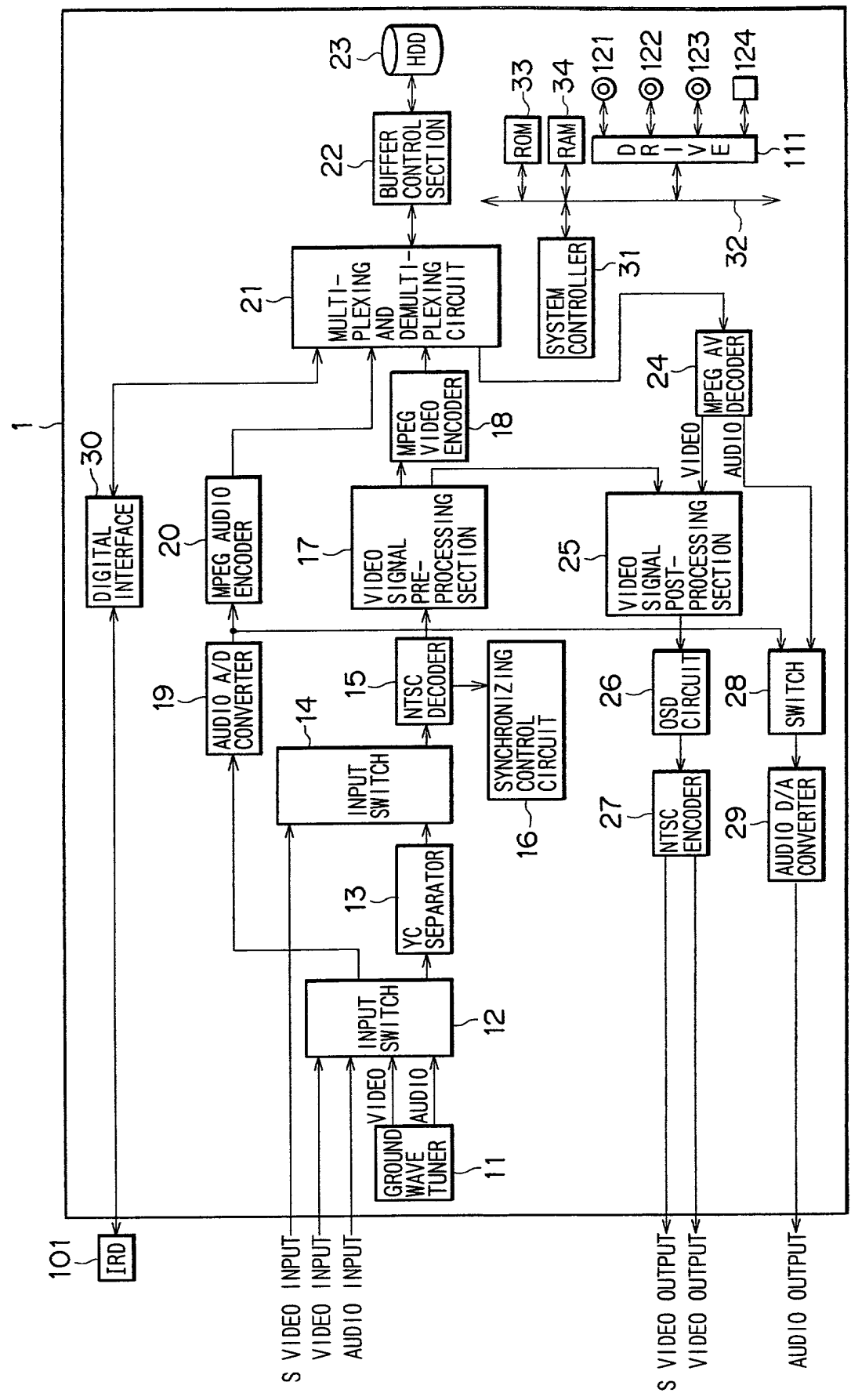


FIG. 2

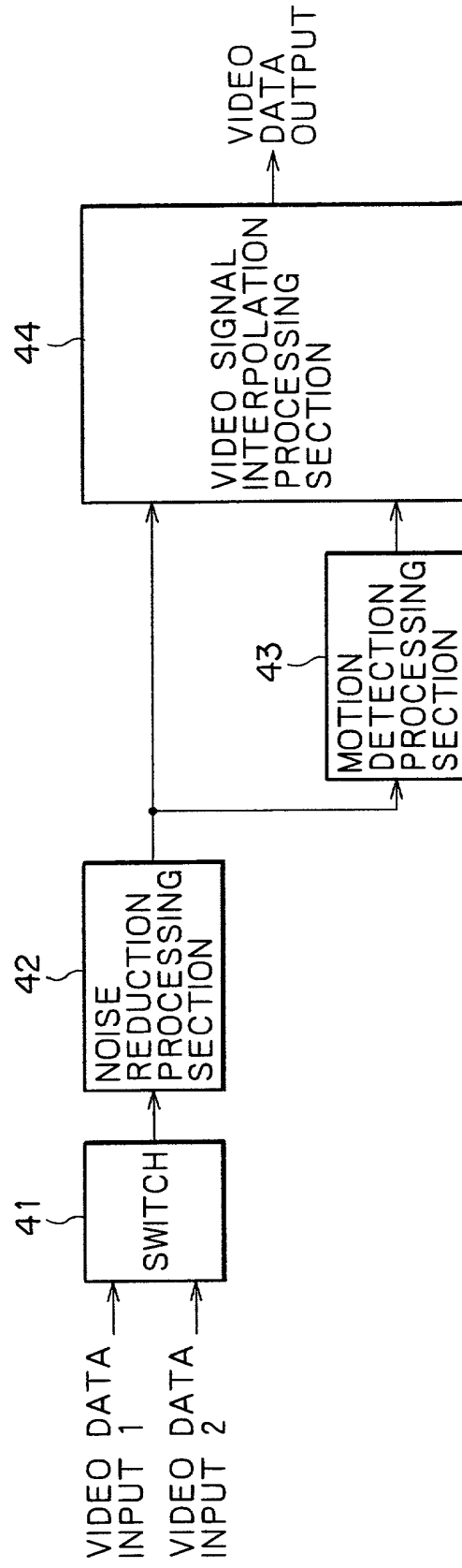


FIG. 3

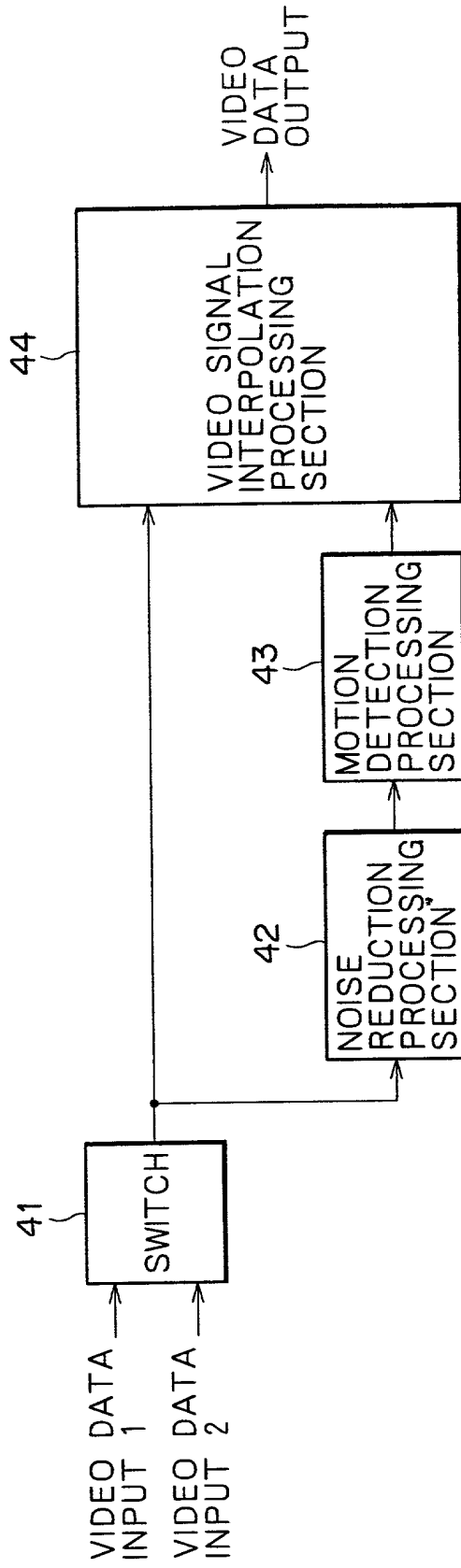


FIG. 4

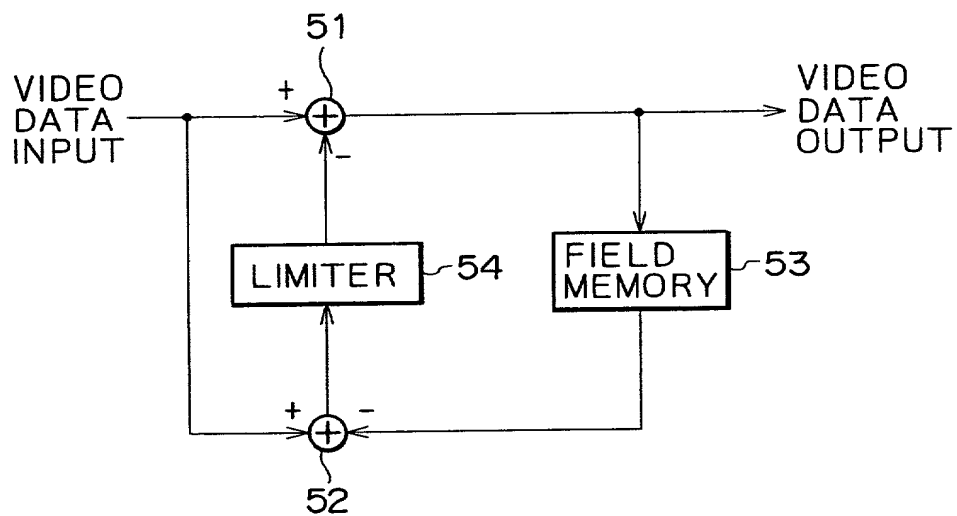


FIG. 5

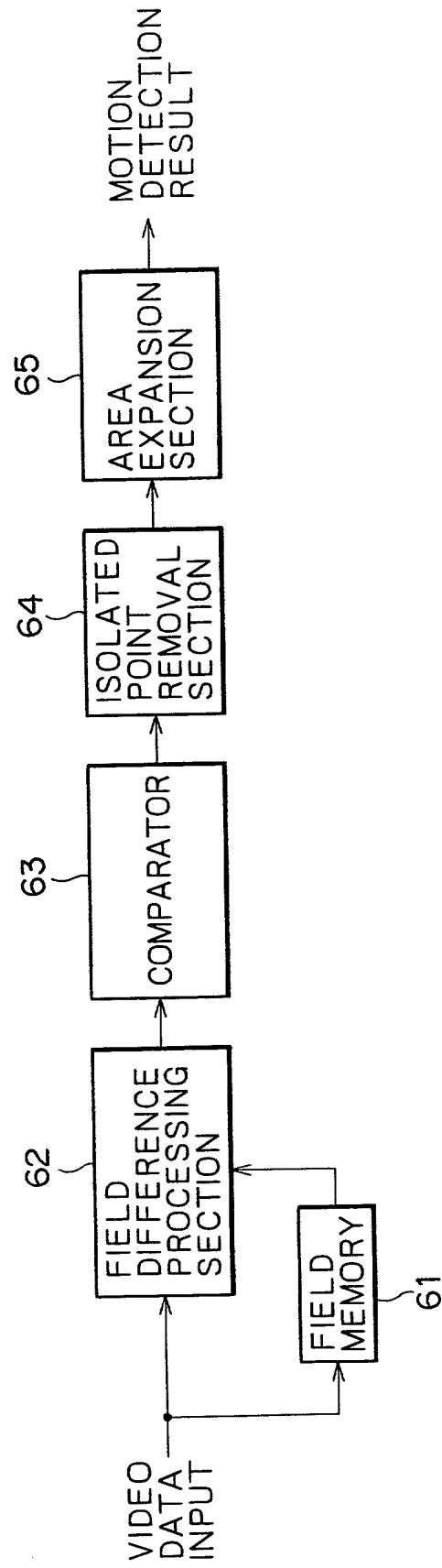


FIG. 6

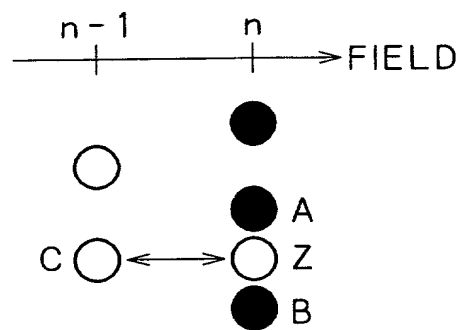


FIG. 7

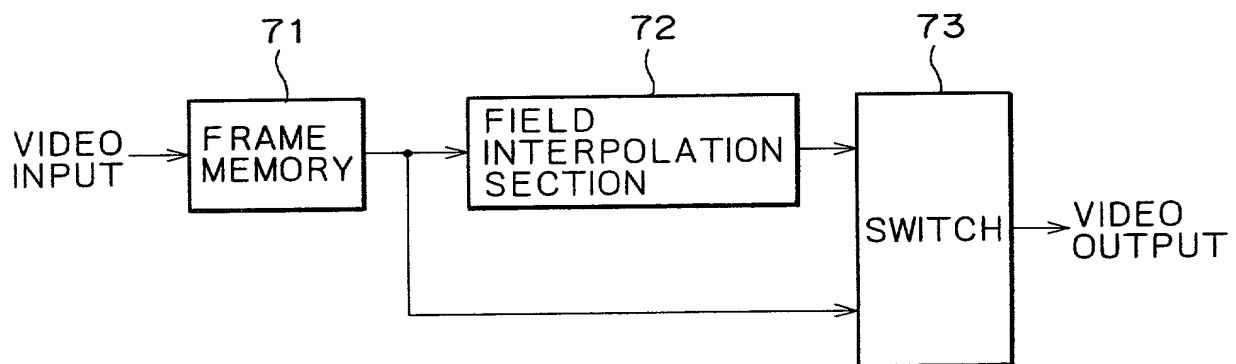


FIG. 8

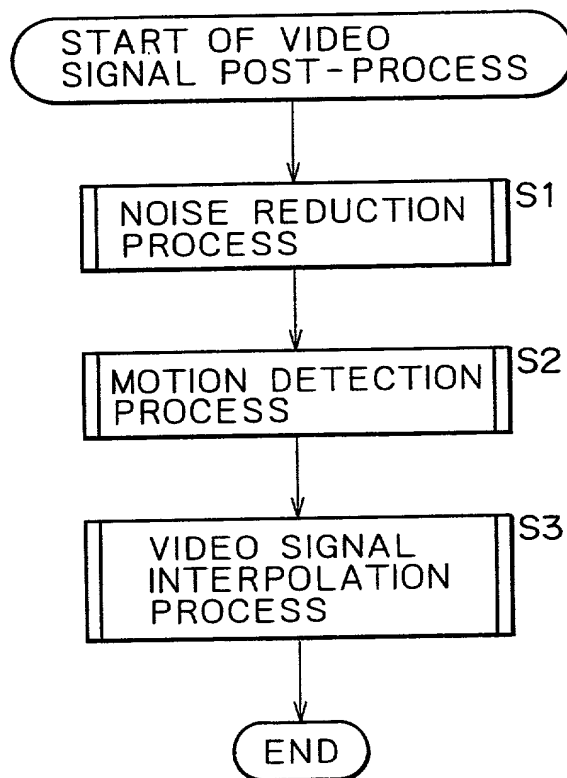


FIG. 9

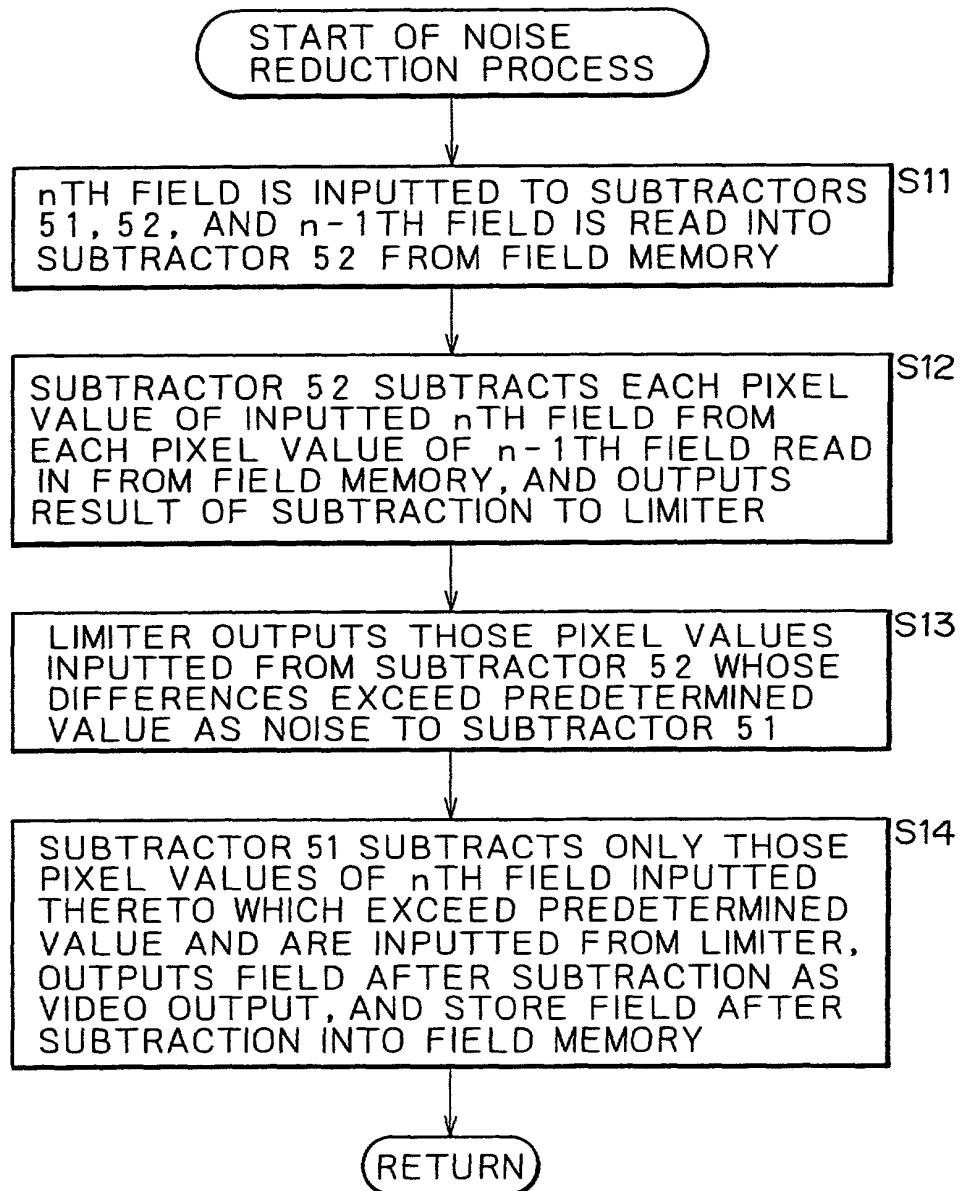


FIG.10

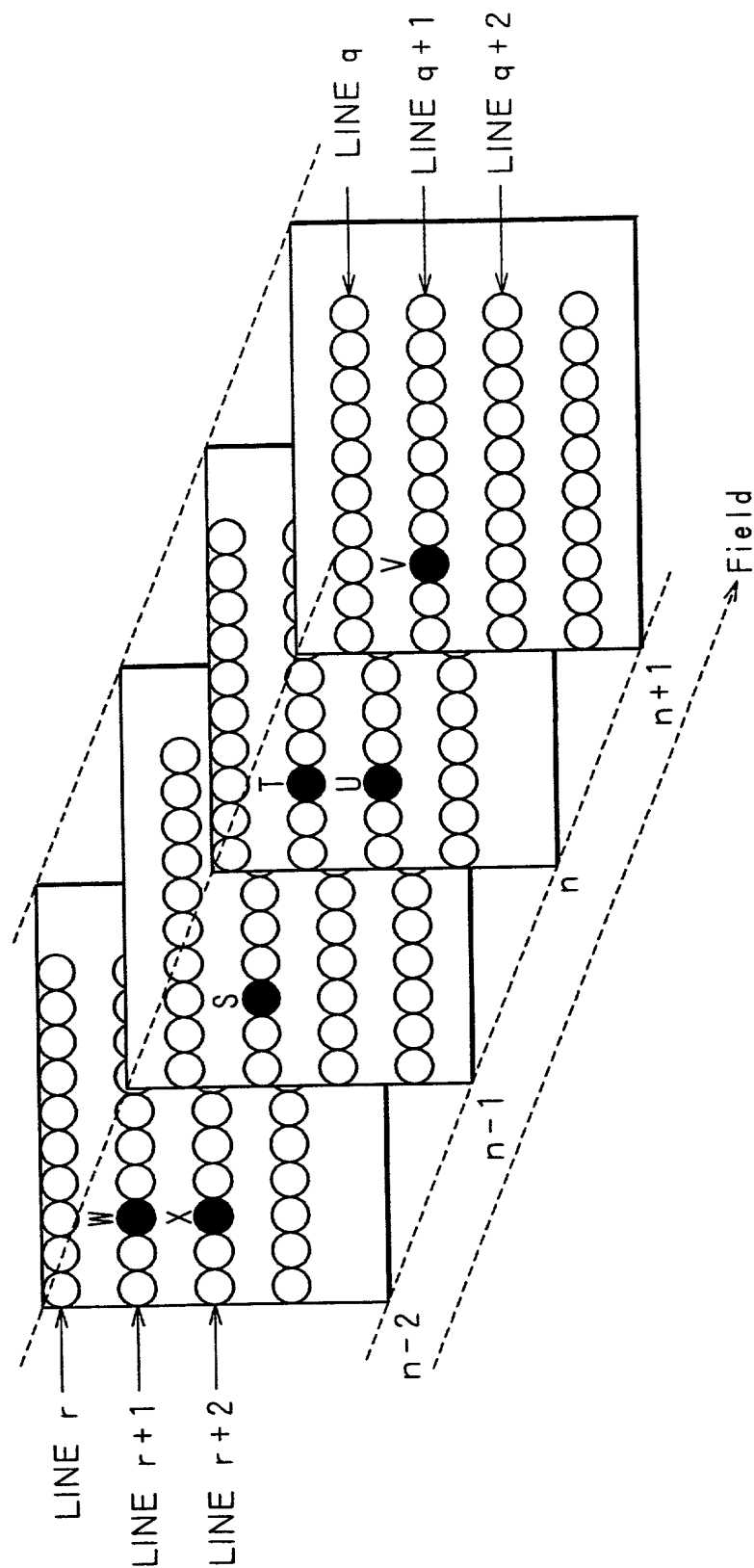


FIG. 11

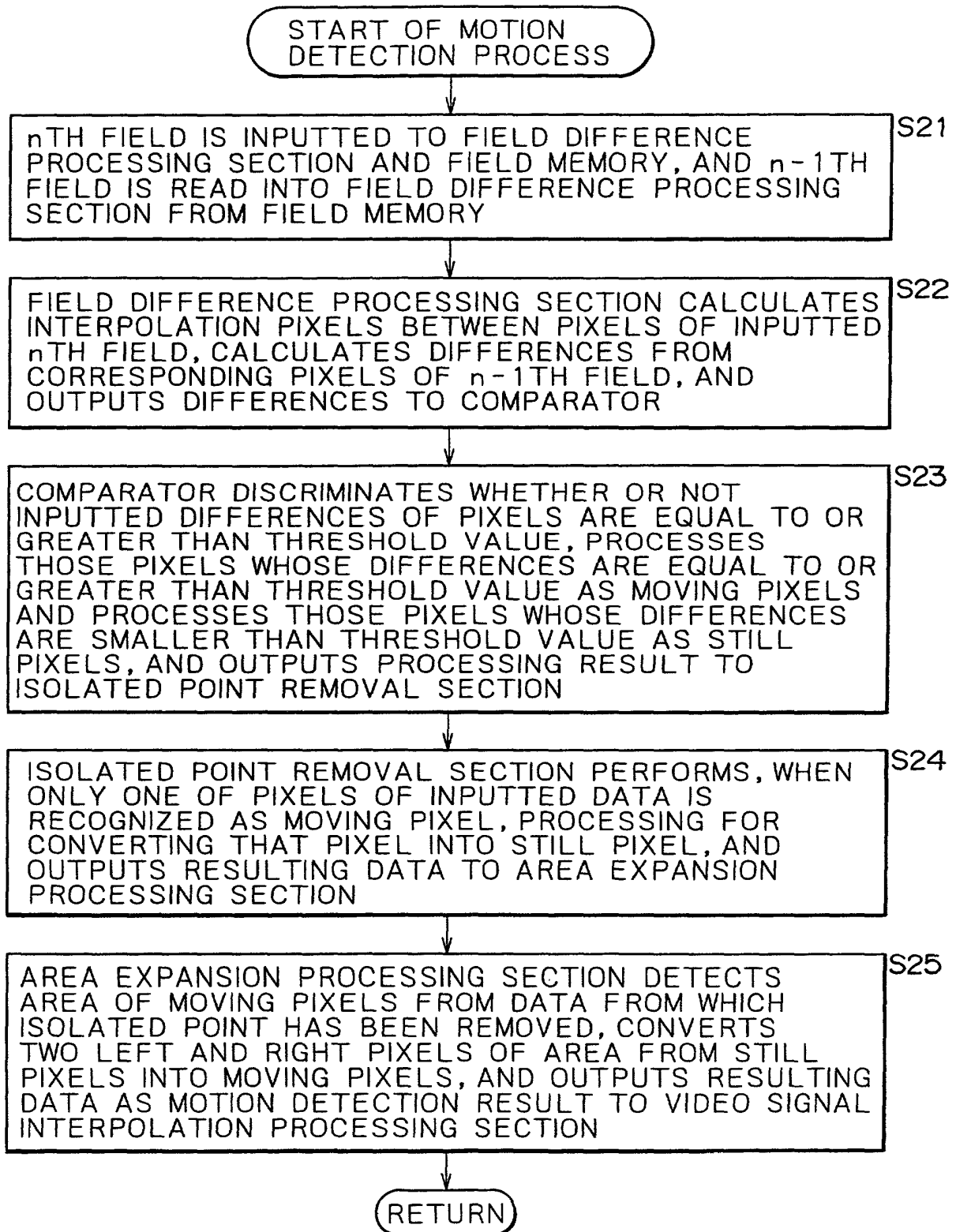


FIG.12

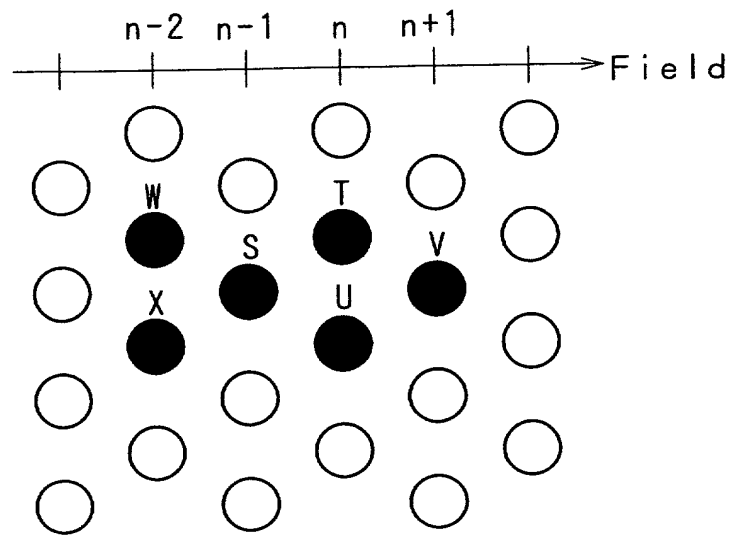


FIG.13

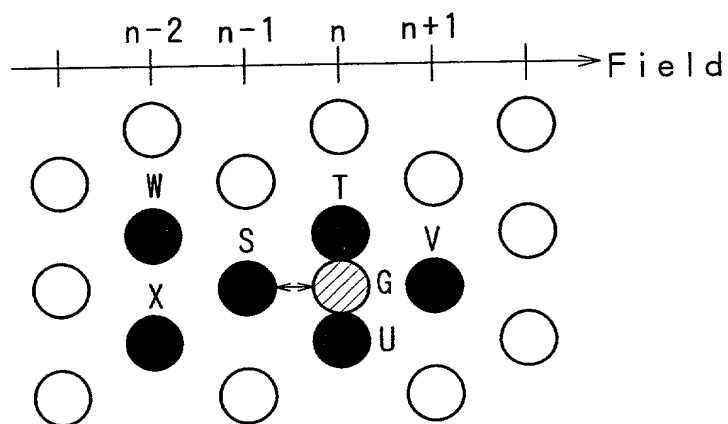


FIG.14A ○●○○●●○○●○
H I J K

FIG.14B ○○○○●●○○○○
H I J K

FIG.15A
 STILL MOVING STILL
 AREA AREA AREA
 ○○○○●●○○○○
 I J

FIG.15B
 STILL MOVING STILL
 AREA AREA AREA
 ○○●●●●●○○○
 I J
 EXPANSION EXPANSION

FIG. 16

